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	-65		140	° C
Tj(FN)	-55		125	° C
VCK VCI1A	-01	11	115	V
VCI1A_FE; VCI1A_AIO VCI1A_CEN; VCI1A_HL	-01	11	115	V
VCI1Q; VCI3A VCI3	-04	33	37	V
VCI1O; VCI25V	-04	33	37	V

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	-40		85	° C
VCK VCI1A	105	11	115	V
VCI1A_FE; VCI1A_AIO VCI1A_CEN; VCI1A_HL	105	11	115	V
VCI1Q; VCI3A VCI3	315	33	345	V
VCI1O; VCI25V	315	33	345	V

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IOreference vdtage	Vref		30	33	36	V
Input low vdtage	Vl				08	V
Input high vdtage	Vh		20			V
Input low current	Iil	Vin=0V	-20		0	μA
Input high current	Iih	Vin=Vref- Vref, max	0		200	μA
Output low vdtage	Vl	Id=-4mA Vref=rin	0		400	mV
Output high vdtage	Vh	ICh=- 4mA Vref=rin	24		Vref	V

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Tck	NSI_REF_CLK Frequency		50		NE
Rdc	NSI_REF_CLK duty cycle	35		65	%
Racc	NSI_REF_CLK accuracy			100	ppm
To	Clock to out (10 pF \times load \leq 50 pF) NSI_EQ1 Q, NSI_SRIV Dta valid from NSI_REF_CLK rising edge	2.5		12.5	ns
Tsu	NSI_EQ1 Q, NSI_TXEN Dta Setup to NSI_CLKIN rising edge	3			ns
Thdd	NSI_EQ1 Q, NSI_TXEN Dta hdd from NSI_REF_CLK rising edge	1			ns
Tr	NSI_EQ1 Q, NSI_SRIV Output Time rise	0.5		6	ns
Tf	NSI_EQ1 Q, NSI_SRIV Output Time fall	0.5		6	ns
Tdr/Tdf	NSI_REF_CLK Rise/Fall Time	0.5		3.5	ns

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Frequency	-	-	25	-	NE
Frequency Stability	Ta=0 70	-30		+30	ppm
Frequency Tolerance	Ta=25	-50		+50	ppm
Duty Cycle		40		60	%
Broadband Peak to peak Jitter				200	ps
Vpeak to peak		3.135	3.3	3.465	V

Rise time 10%90%				10	ns
Fall time 10%90%				10	ns
Operation temperature Range		0		70	

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CHY IP 1 IV 33V 5ms 33V rise time 1ms
33V 1 IV

Rt1	33V rise time	1	-	100	ms
Rt2	33V ready to 1 IV ready time	-5	-	-	ms

vrbord	V5Q0V
microchip	SS125AF080B
	CD5Q0

1	VN8002		0 - 70 , 4m2	2
2	VN8002S		0 - 70 , 4m2 , SM/SN/SM	2
3	VN8004		0 - 70 , 4m4	4
4	VN8004S		0 - 70 , 4m4 , SM/SN/SM	4
5	VN8002L2		-40 - 85 , 4m2	2
6	VN8002LS		-40 - 85 , 4m2 , SM/SN/SM	2
7	VN8004L4		-40 - 85 , 4m4	4
8	VN8004LS		-40 - 85 , 4m4 , SM/SN/SM	4

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